FIG.1

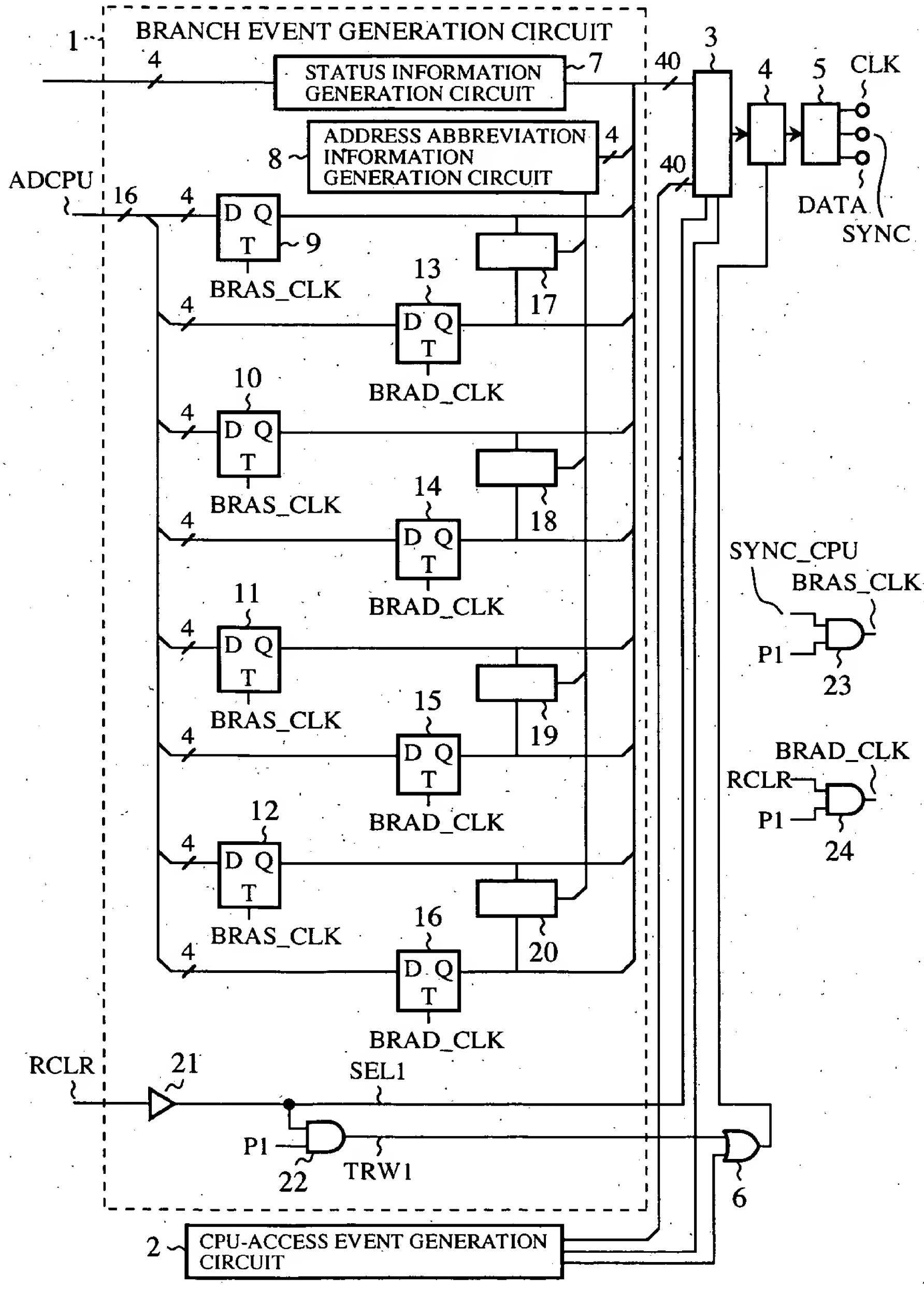

BRANCH EVENT GENERATION CIRCUIT
1
4
STATUS INFORMATION GENERATION CIRCUIT
7
40
3
4
5
CLK
DATA
SYNC
ADDRESS ABBREVIATION INFORMATION GENERATION CIRCUIT
8
4
40
ADCPU
16
4
D Q
T
9
BRAS_CLK
13
17
BRAD_CLK
10
14
18
11
15
19
12
16
20
SYNC_CPU
BRAS_CLK
P1
23
BRAD_CLK
RCLR
P1
24
RCLR
21
SEL1
P1
22
TRW1
6
2
CPU-ACCESS EVENT GENERATION CIRCUIT

FIG.2

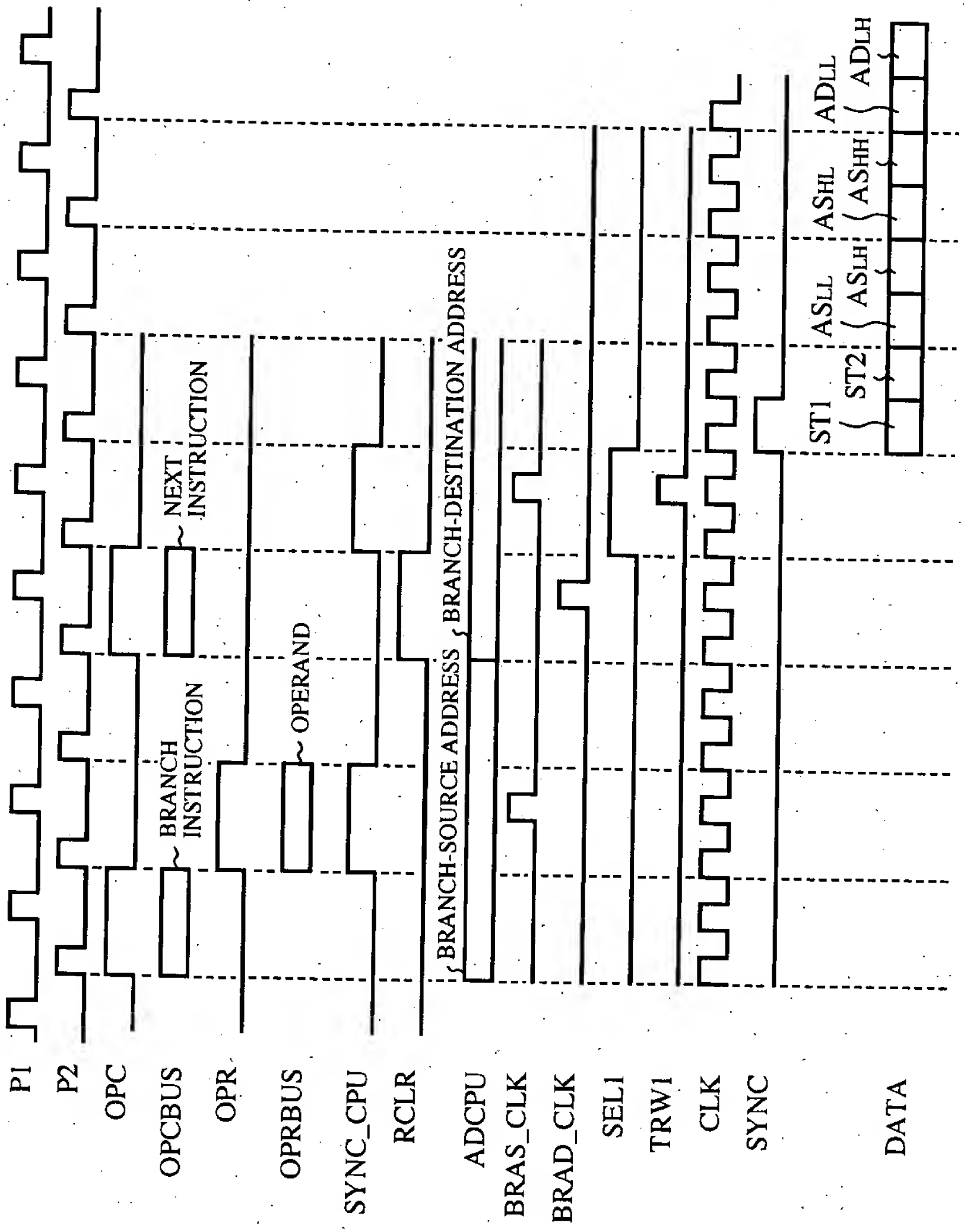

P1
P2
OPC
OPCBUS
OPR
OPRBUS
SYNC_CPU
RCLR
ADCPU
BRAS_CLK
BRAD_CLK
SEL1
TRW1
CLK
SYNC
DATA
BRANCH INSTRUCTION
NEXT INSTRUCTION
OPERAND
BRANCH-SOURCE ADDRESS
BRANCH-DESTINATION ADDRESS
ST1
ST2
ASLL
ASLH
ASHL
ASHH
ADLL
ADLH

FIG.3

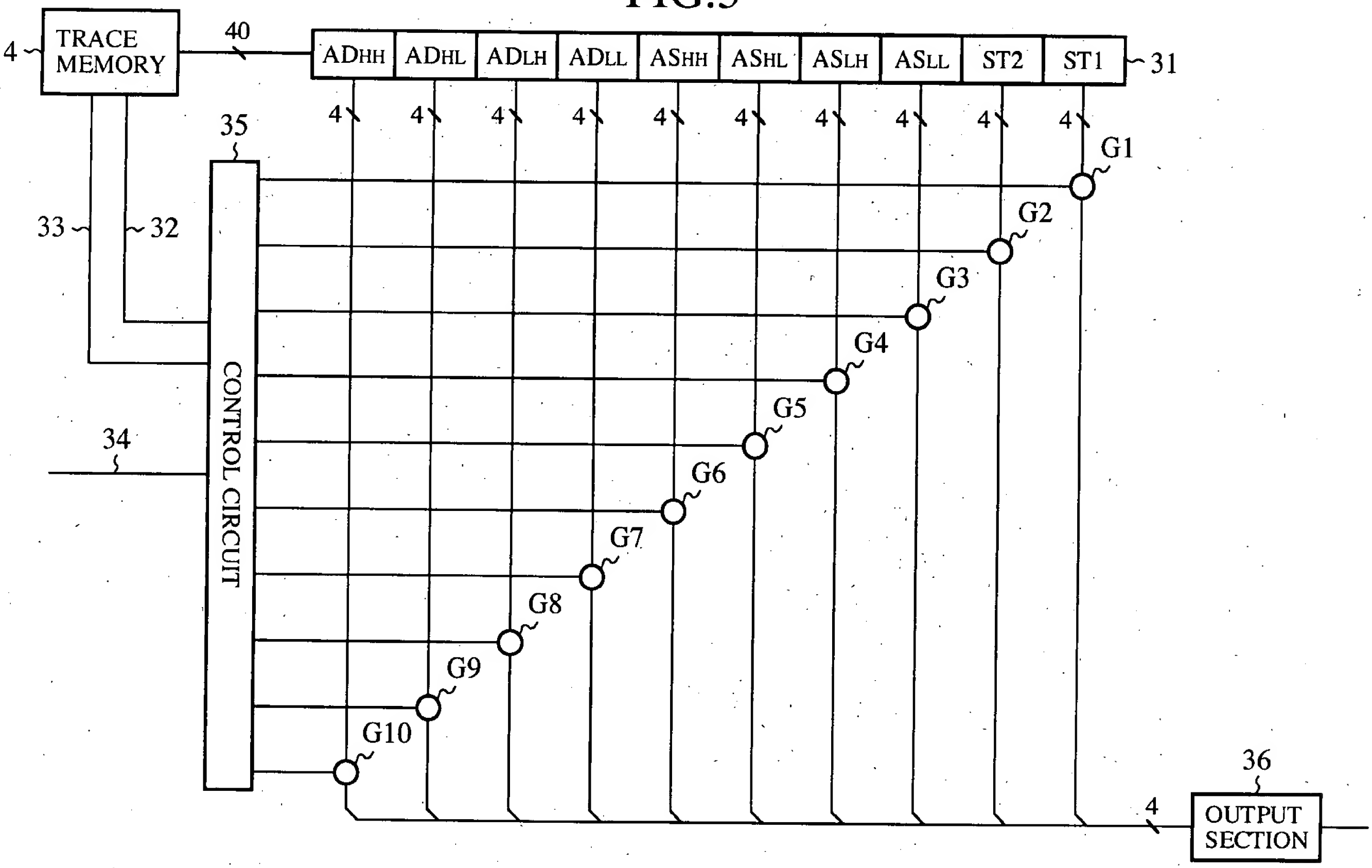

TRACE MEMORY
4
40
ADHH
ADHL
ADLH
ADLL
ASHH
ASHL
ASLH
ASLL
ST2
ST1
31
4
35
33
32
34
CONTROL CIRCUIT
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
36
OUTPUT SECTION

FIG.4

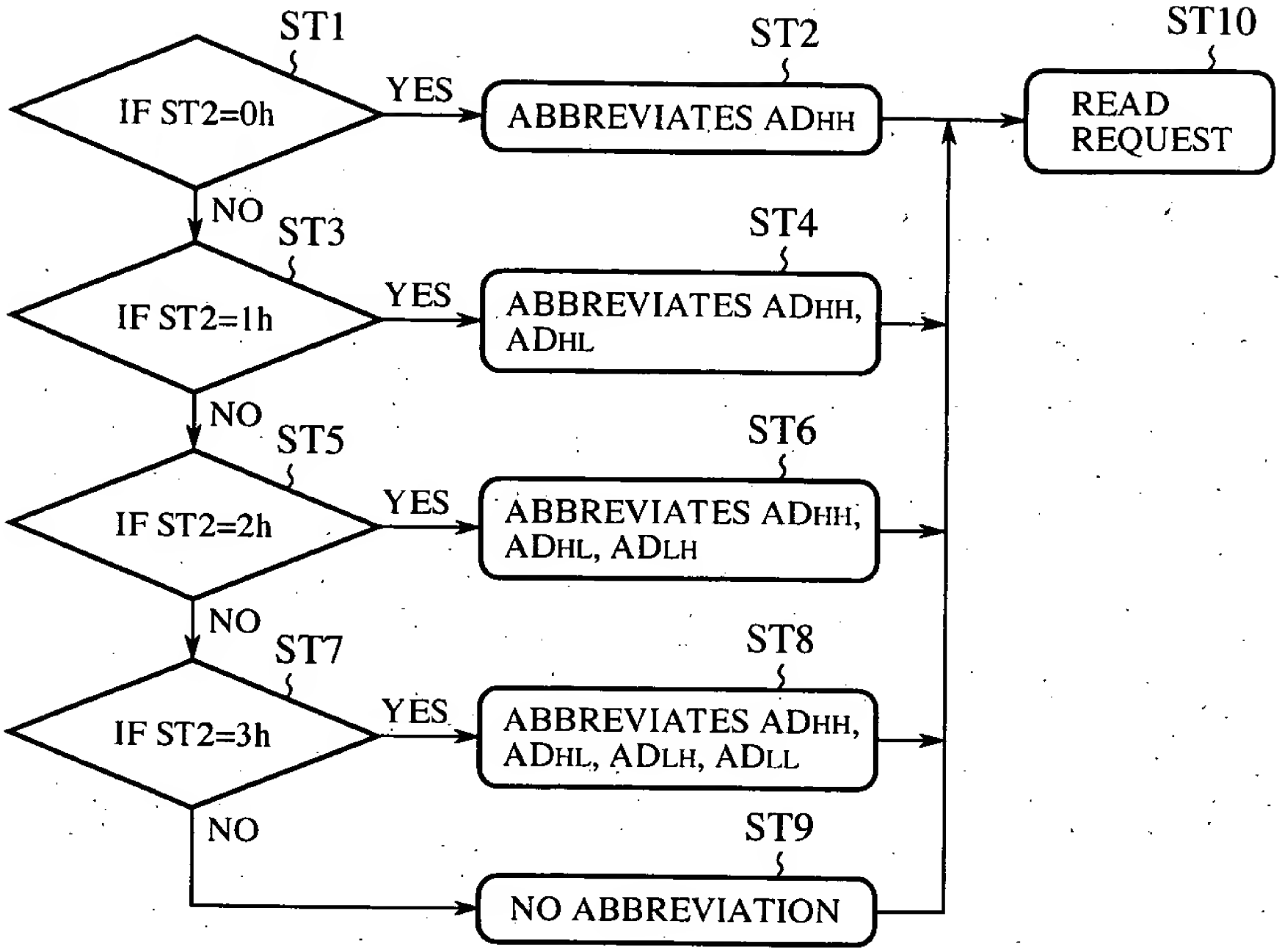

ST1
IF ST2=0h
YES
ST2
ABBREVIATES ADHH
ST10
READ REQUEST
NO
ST3
IF ST2=1h
YES
ST4
ABBREVIATES ADHH, ADHL
NO
ST5
IF ST2=2h
YES
ST6
ABBREVIATES ADHH, ADHL, ADLH
NO
ST7
IF ST2=3h
YES
ST8
ABBREVIATES ADHH, ADHL, ADLH, ADLL
NO
ST9
NO ABBREVIATION

FIG.5

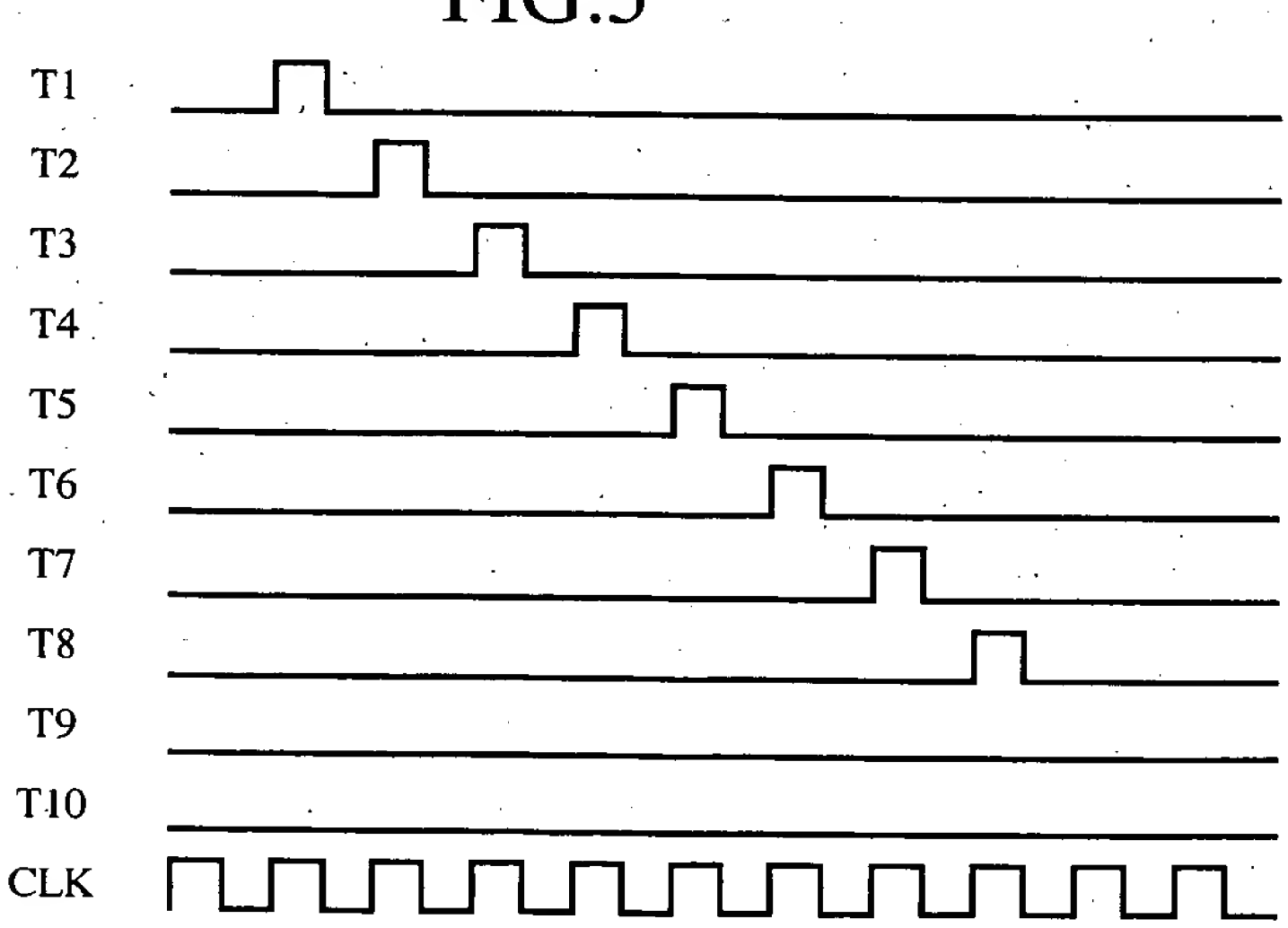

T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CLK

FIG.6

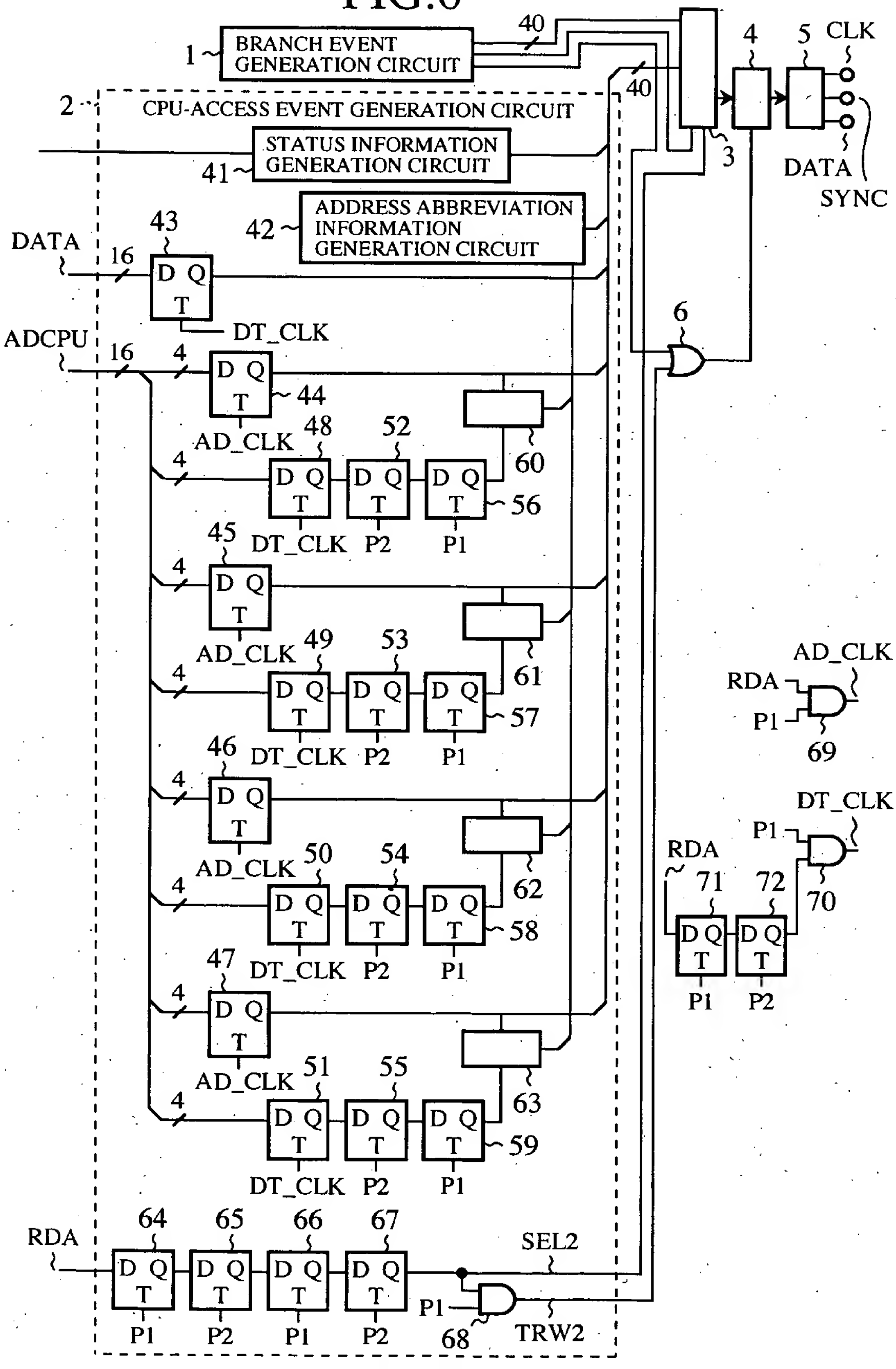

1
BRANCH EVENT GENERATION CIRCUIT
40
2
CPU-ACCESS EVENT GENERATION CIRCUIT
STATUS INFORMATION GENERATION CIRCUIT
41
ADDRESS ABBREVIATION INFORMATION GENERATION CIRCUIT
42
43
DATA
16
D Q T
DT_CLK
ADCPU
16
4
44
AD_CLK
48
52
60
56
DT_CLK P2 P1
45
49
53
61
57
46
50
54
62
58
47
51
55
63
59
64
65
66
67
RDA
SEL2
P1
68
TRW2
4
5
CLK
DATA
SYNC
3
6
AD_CLK
RDA
P1
69
DT_CLK
71
72
70

FIG.7

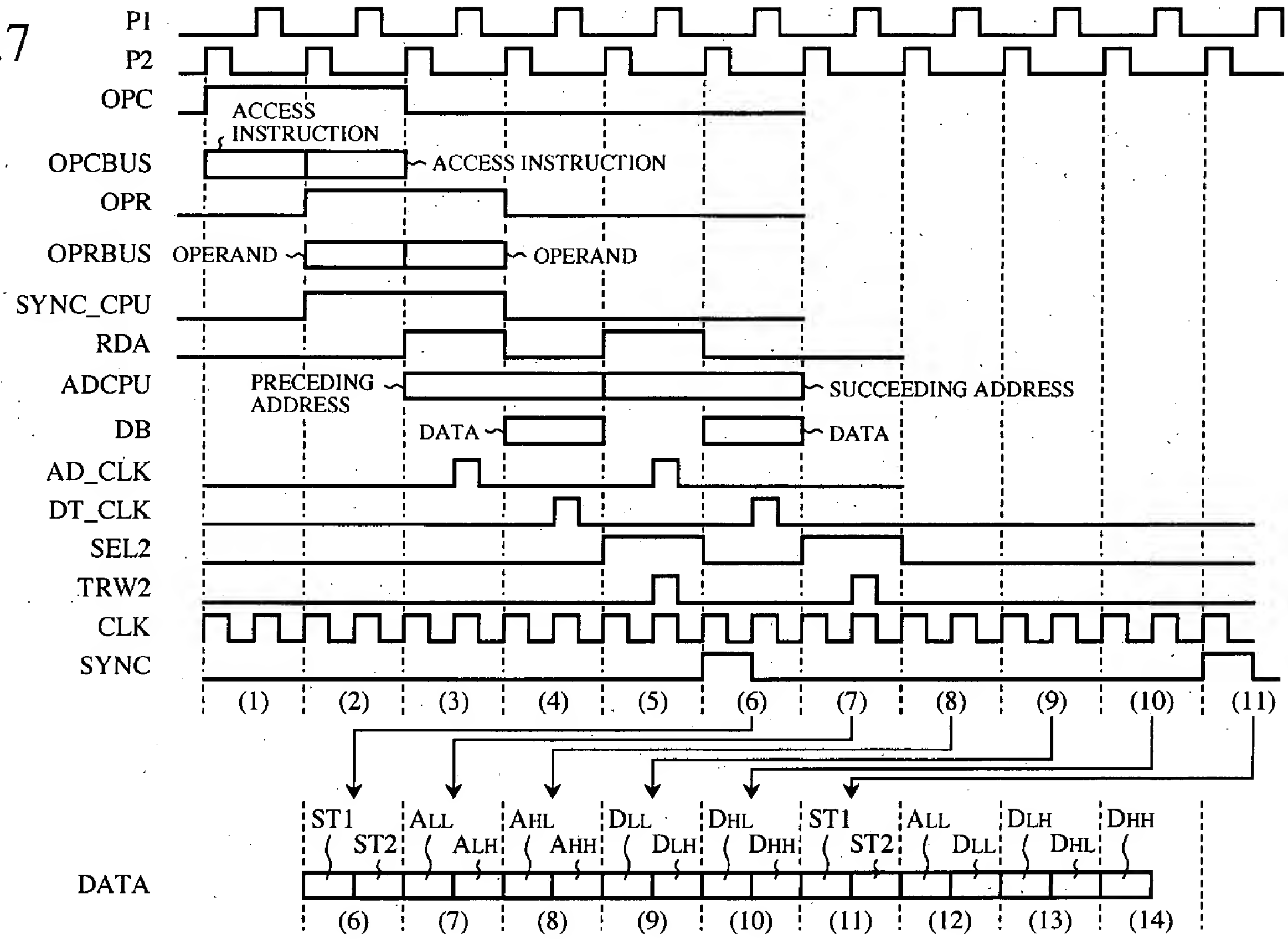

P1
P2
OPC
ACCESS INSTRUCTION
OPCBUS
ACCESS INSTRUCTION
OPR
OPRBUS
OPERAND
OPERAND
SYNC_CPU
RDA
ADCPU
PRECEDING ADDRESS
SUCCEEDING ADDRESS
DB
DATA
DATA
AD_CLK
DT_CLK
SEL2
TRW2
CLK
SYNC
(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11)
ST1 ST2 ALL ALH AHL AHH DLL DLH DHL DHH ST1 ST2 ALL DLL DLH DHL DHH
DATA
(6) (7) (8) (9) (10) (11) (12) (13) (14)

FIG.8

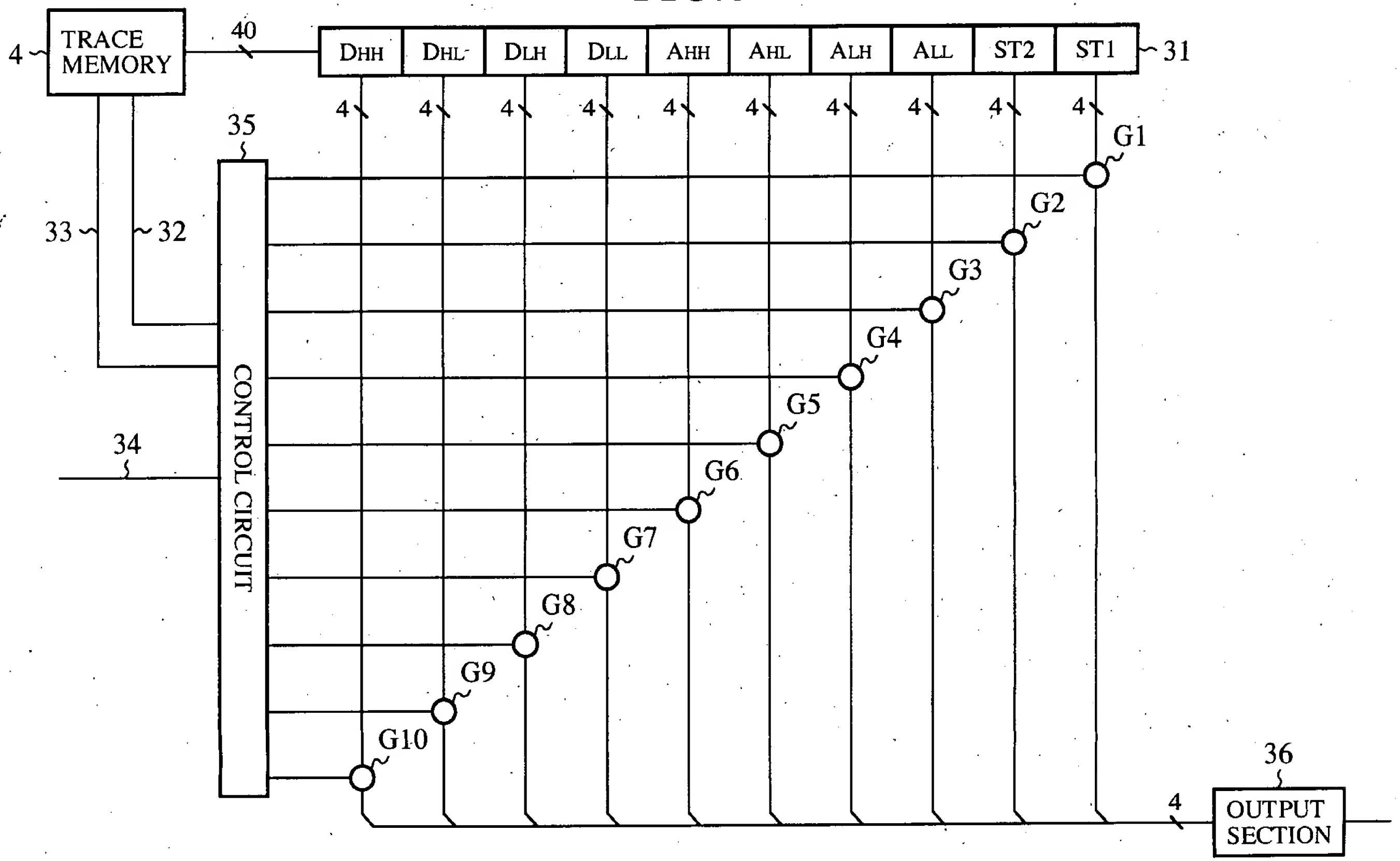

TRACE MEMORY
4
40
DHH
DHL
DLH
DLL
AHH
AHL
ALH
ALL
ST2
ST1
31
4
35
33
32
34
CONTROL CIRCUIT
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
36
OUTPUT SECTION

FIG.9

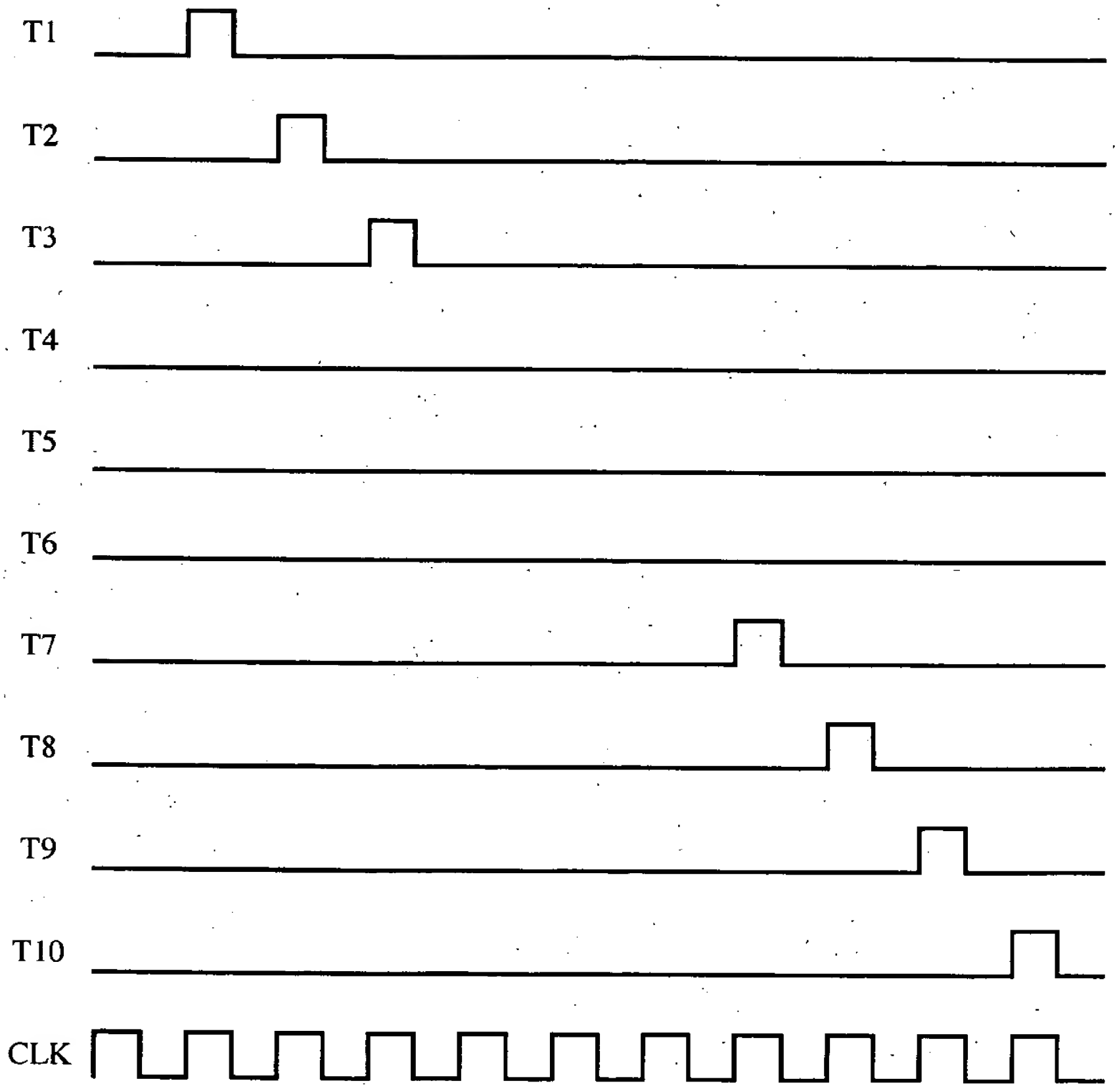


FIG.10

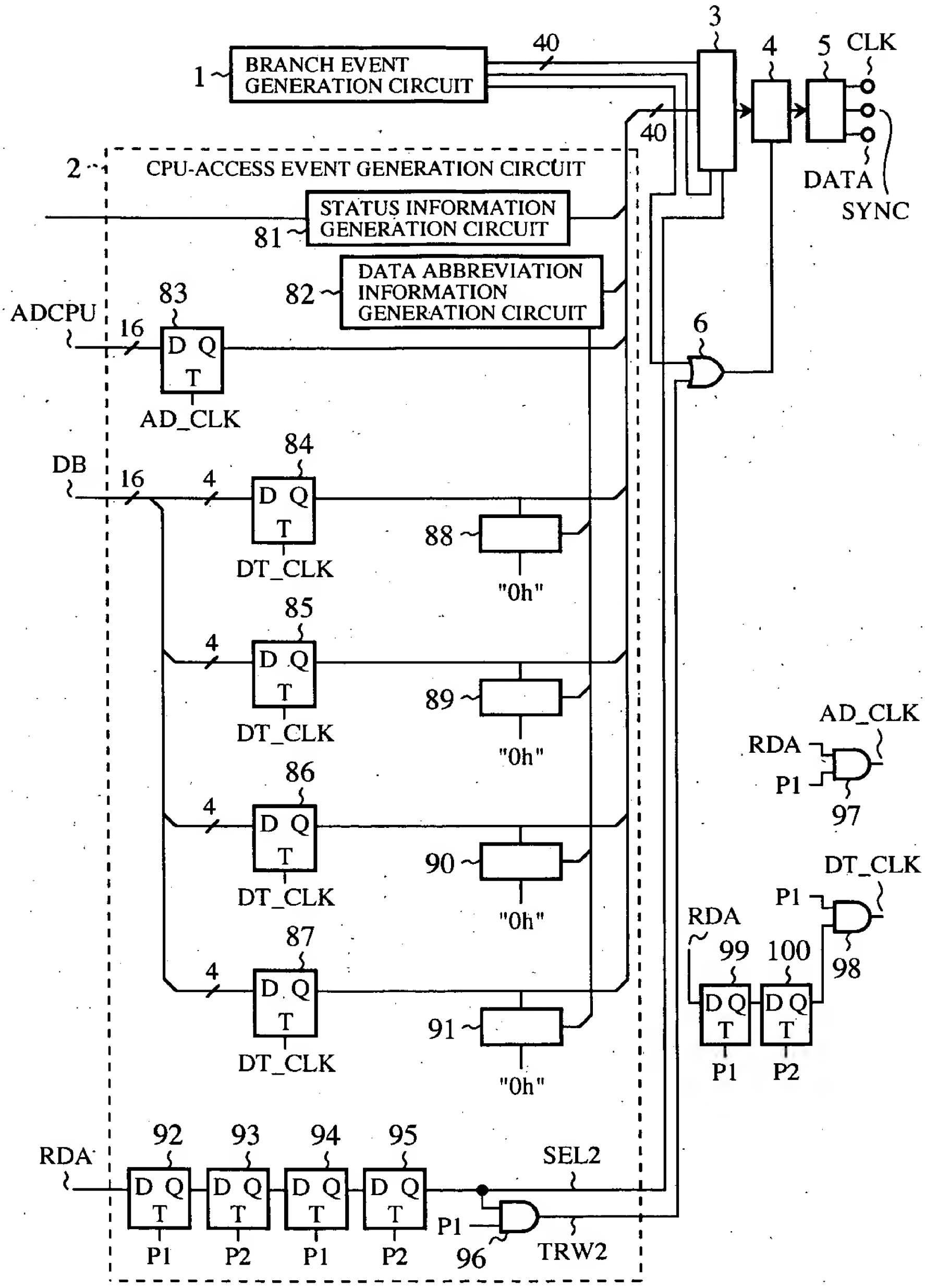

1
BRANCH EVENT GENERATION CIRCUIT
40
3
4
5
CLK
DATA
SYNC
40
2
CPU-ACCESS EVENT GENERATION CIRCUIT
81
STATUS INFORMATION GENERATION CIRCUIT
82
DATA ABBREVIATION INFORMATION GENERATION CIRCUIT
6
ADCPU
16
83
D Q
T
AD_CLK
DB
16
4
84
D Q
T
DT_CLK
88
"0h"
4
85
D Q
T
DT_CLK
89
"0h"
4
86
D Q
T
DT_CLK
90
"0h"
4
87
D Q
T
DT_CLK
91
"0h"
RDA
92
93
94
95
D Q
T
P1
P2
P1
P2
SEL2
P1
96
TRW2
AD_CLK
RDA
P1
97
DT_CLK
P1
RDA
99
100
98
D Q
T
P1
P2

FIG.11

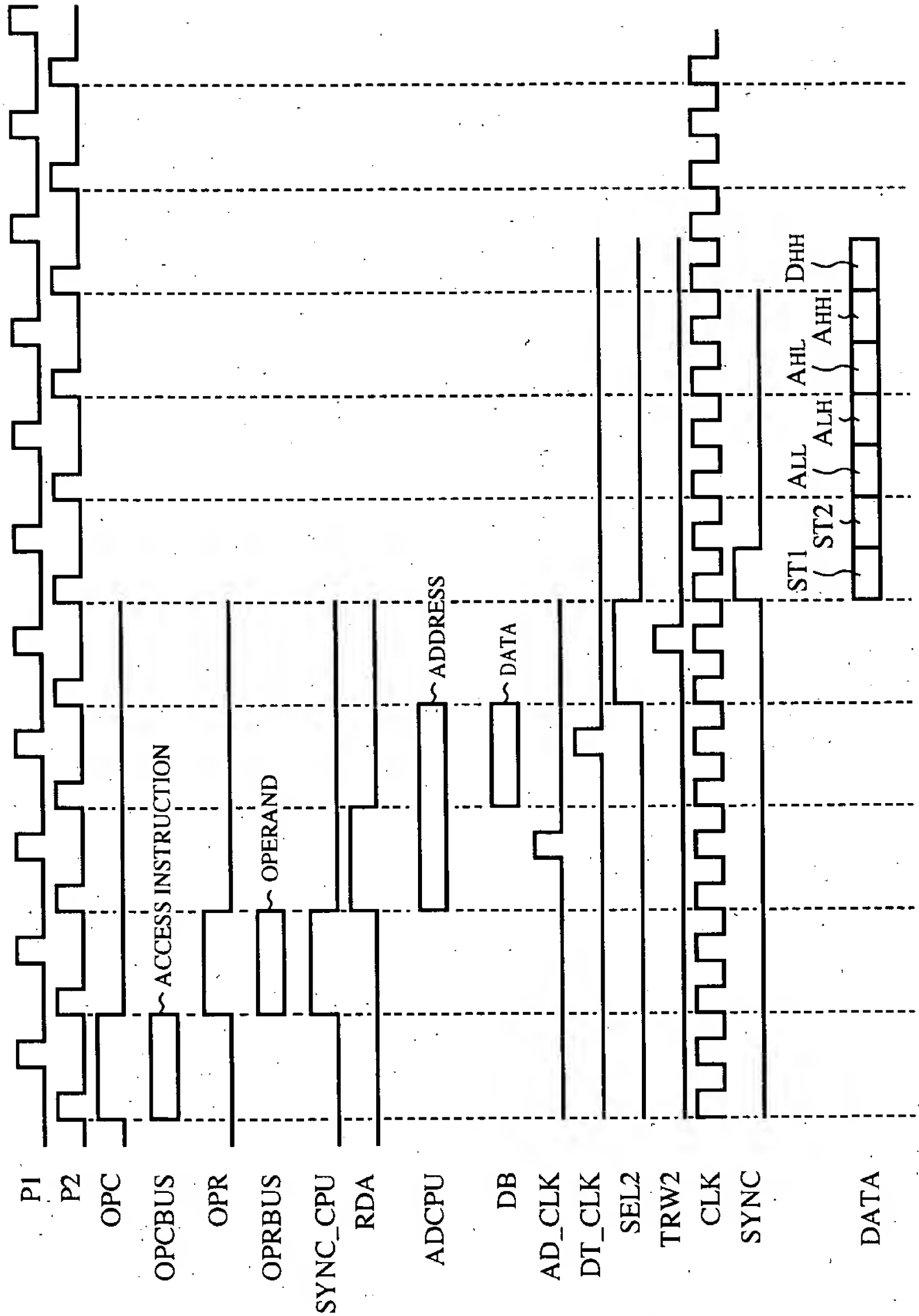

P1
P2
OPC
OPCBUS
OPR
OPRBUS
SYNC_CPU
RDA
ADCPU
DB
AD_CLK
DT_CLK
SEL2
TRW2
CLK
SYNC
DATA
ACCESS INSTRUCTION
OPERAND
ADDRESS
DATA
ST1
ST2
ALL
ALH
AHL
AHH
DHH

FIG.12

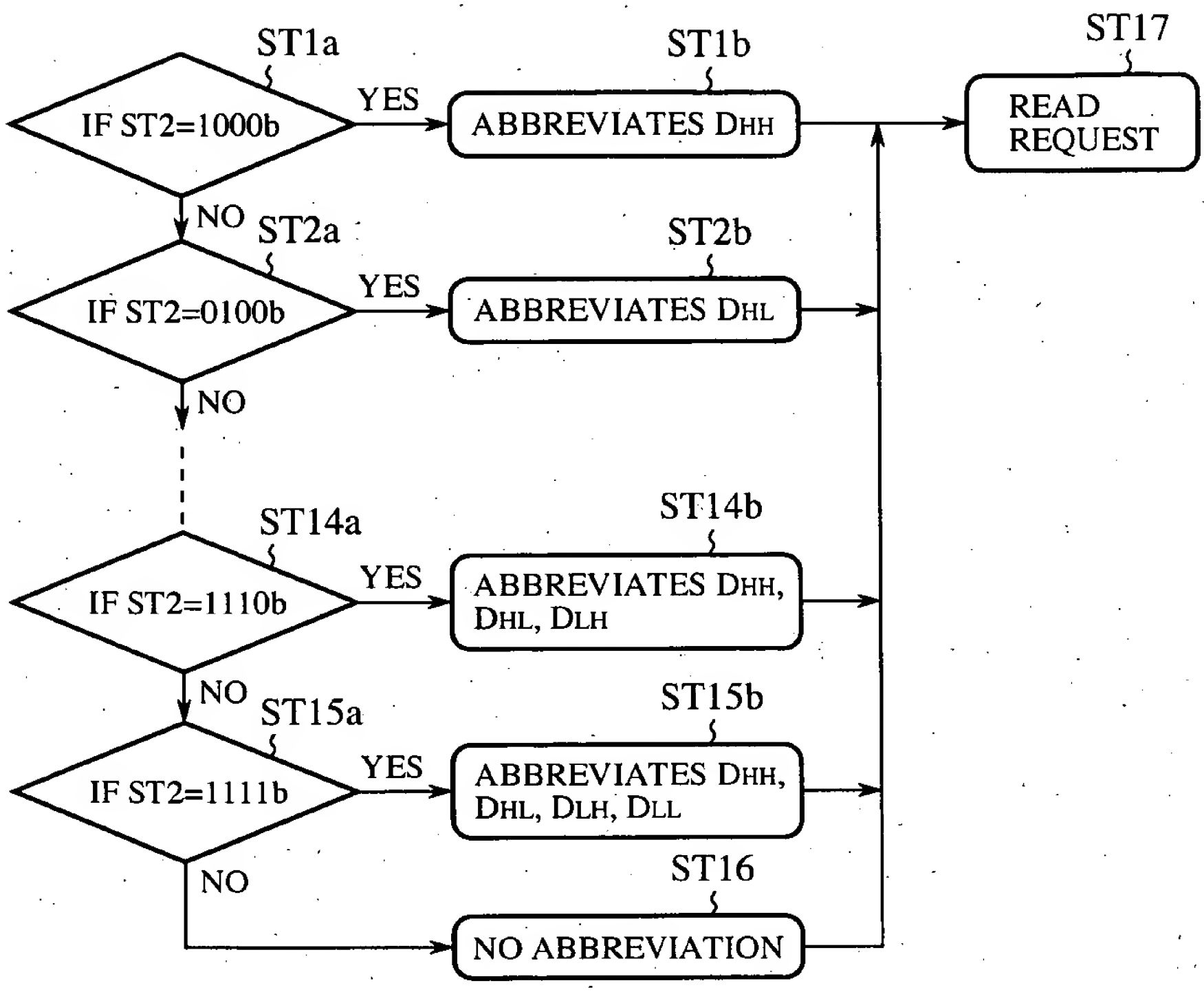
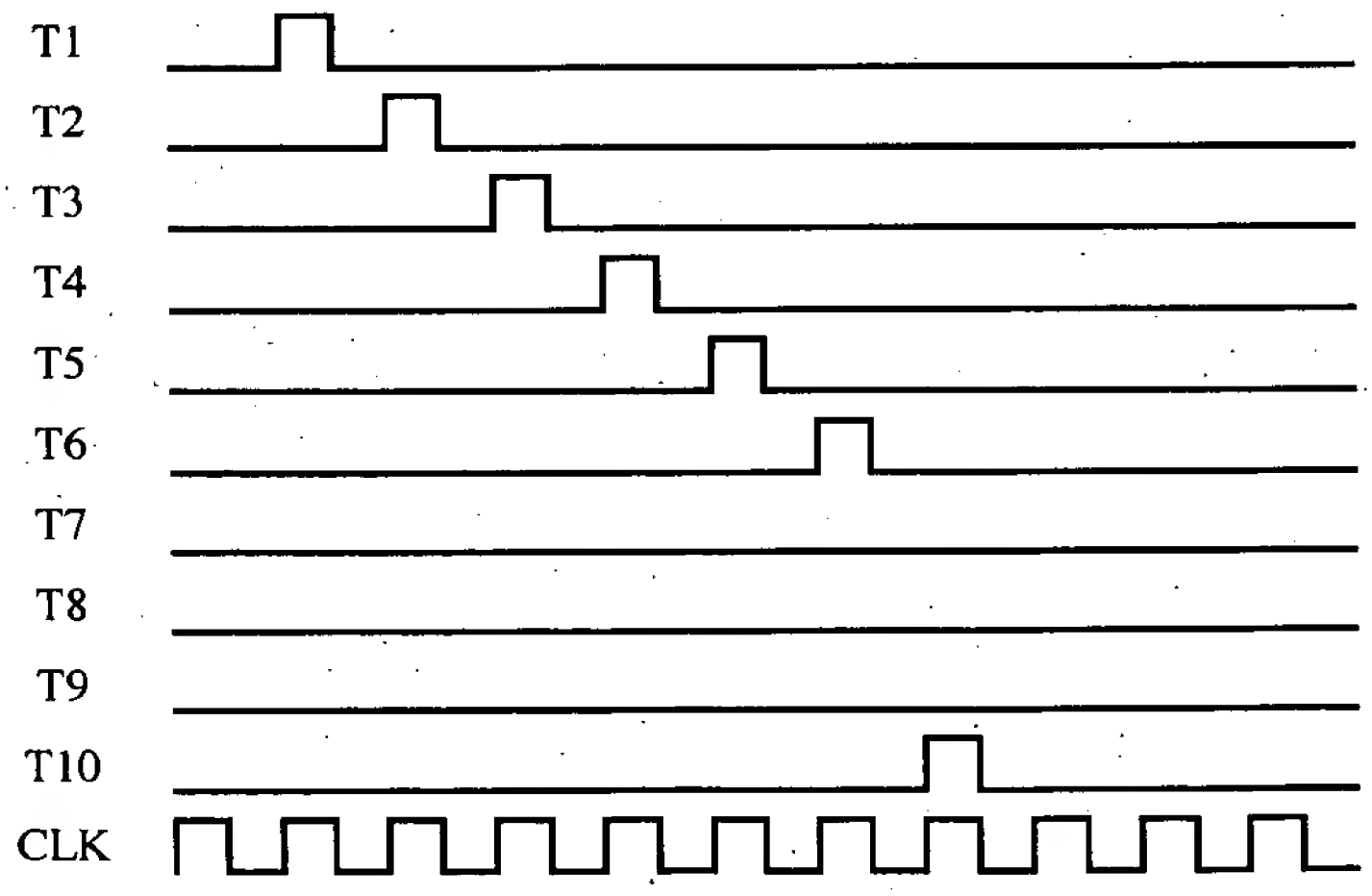

ST1a
IF ST2=1000b
YES
ST1b
ABBREVIATES DHH
ST17
READ REQUEST
NO
ST2a
IF ST2=0100b
YES
ST2b
ABBREVIATES DHL
NO
ST14a
IF ST2=1110b
YES
ST14b
ABBREVIATES DHH, DHL, DLH
NO
ST15a
IF ST2=1111b
YES
ST15b
ABBREVIATES DHH, DHL, DLH, DLL
NO
ST16
NO ABBREVIATION

FIG.13


T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CLK

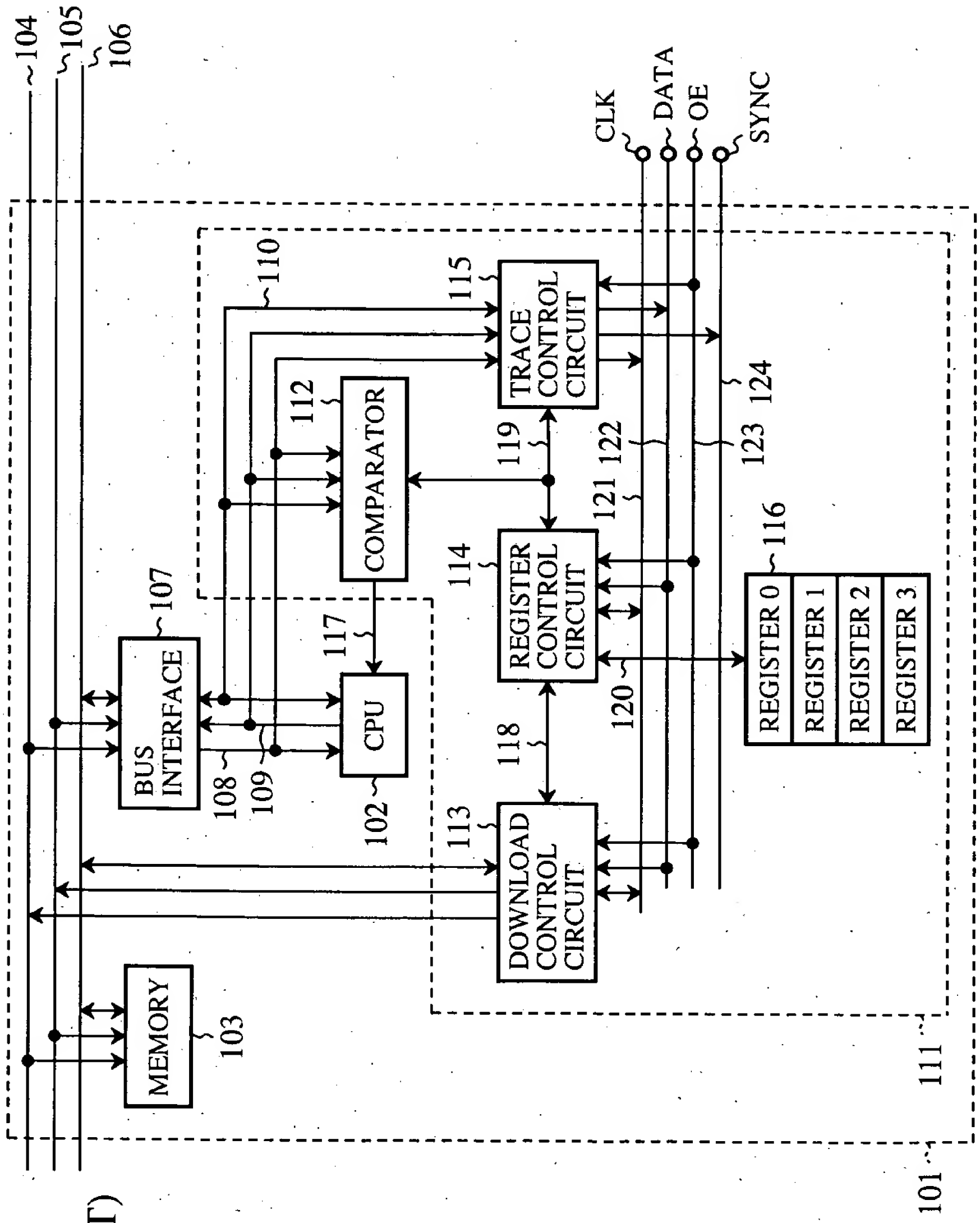


FIG.14
(PRIOR ART)

FIG.15 (PRIOR ART)

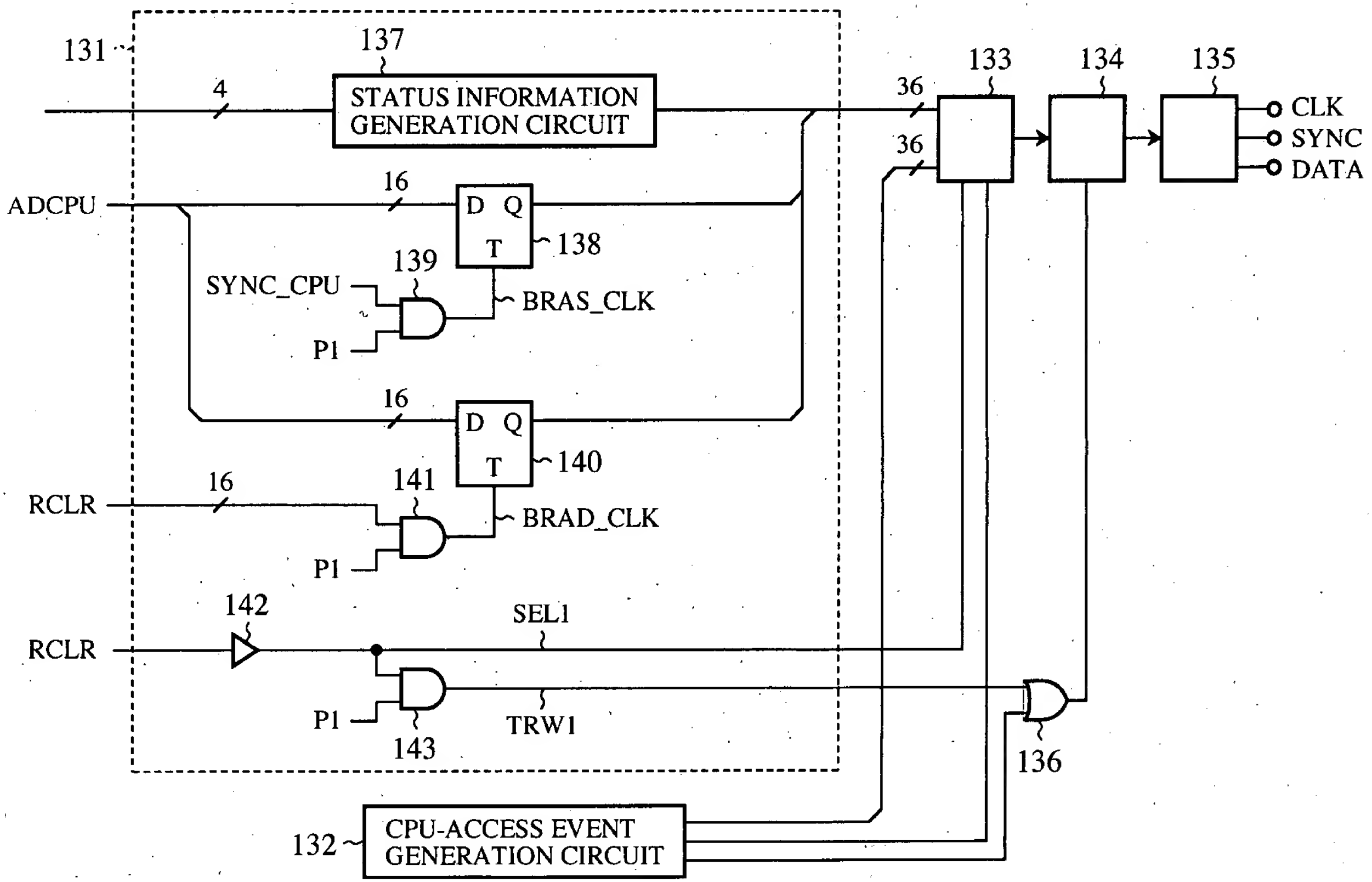


FIG.16 (PRIOR ART)

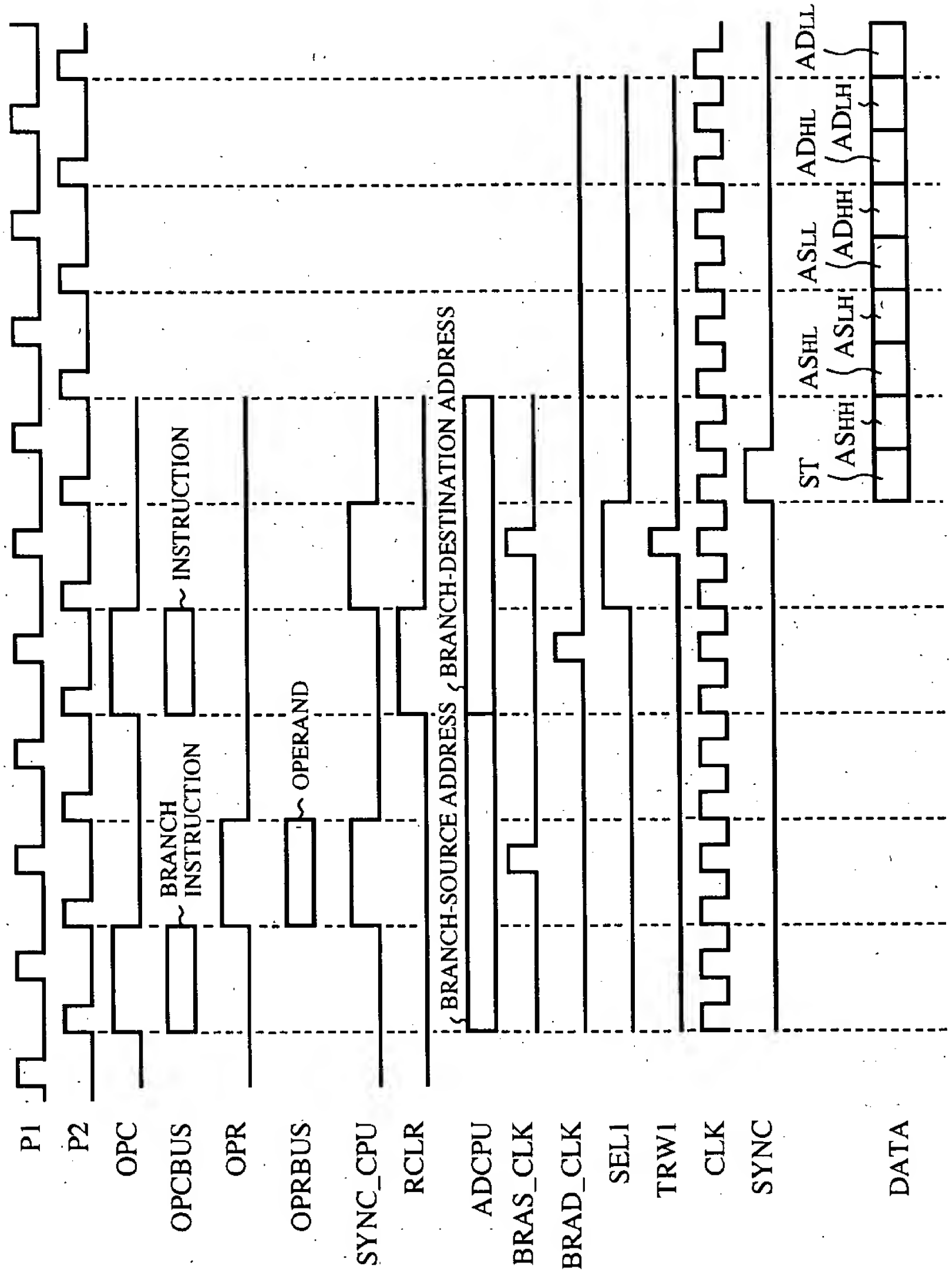


FIG.17
(PRIOR ART)

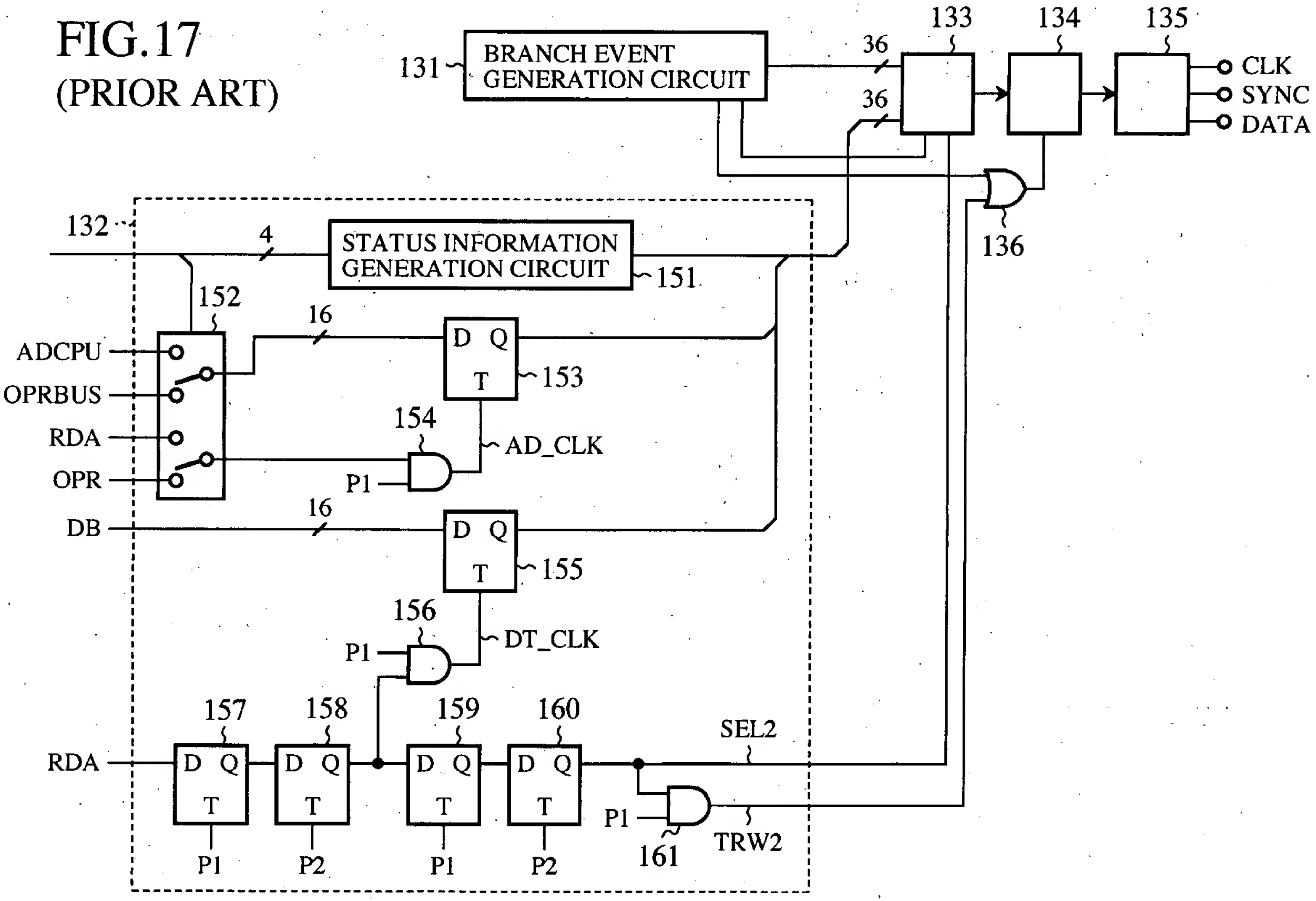


FIG.18 (PRIOR ART)